CLAIMS

WHAT IS CLAIMED IS:

1. A method for decoding a low density parity check (LDPC) coded signal, the method comprising:

retrieving edge values associated with a structured parity check matrix used to generate the LDPC coded signal, wherein the edge values specify relationship of bit nodes and check nodes, and are stored according to a predetermined scheme that permits concurrent retrieval of a set of the edge values; and

outputting a decoded signal corresponding to the LDPC coded signal based on the retrieved edge values.

2. A method according to claim 1, wherein the edge values in the retrieving step are stored in memory according to the predetermined scheme, and the predetermined scheme specifies contiguous physical memory locations for the set of edge values.

3. A method according to claim 2, wherein the memory is partitioned according to degrees of the bit nodes.

4. A method according to claim 3, wherein edge values having bit nodes of n degrees are stored in a first portion of the memory, and edge values having bit nodes of greater than n degrees are stored in a second portion of the memory.

5. A method according to claim 2, wherein addresses of the memory is stored in a Read-Only memory.

6. A method according to claim 2, wherein the set of edge values is retrieved in a single clock cycle of a processor coupled to the memory, and is adjacent to a group of M bit nodes or M check nodes, where M is the number of parallel processing engines.

7. A method according to claim 2, wherein the contiguous placement of edges imposes restrictions on the parity check matrix.

8. A method according to claim 1, wherein the LDPC coded signal is modulated according to a signal constellation that includes one of 8-PSK (Phase Shift Keying), 16-QAM (Quadrature Amplitude Modulation), 16-APSK (Amplitude Phase Shift Keying), 32-APSK and QPSK (Quadrature Phase Shift Keying).

9. A method according to claim 1, wherein the set of edge values in the retrieving step is of a fixed size.

10. A computer-readable medium bearing instructions decoding a low density parity check (LDPC) coded signal, said instruction, being arranged, upon execution, to cause one or more processors to perform the method of claim 1.

11. A decoder for decoding a low density parity check (LDPC) coded signal, comprising:

means for retrieving edge values associated with a structured parity check matrix used to generate the LDPC coded signal;

memory for storing the edge values according to a predetermined scheme that permits concurrent retrieval of a set of the edge values, wherein the edge values specify relationship of bit nodes and check nodes; and

means for outputting a decoded signal corresponding to the LDPC coded signal based on the retrieved edge values.

12. A decoder according to claim 11, wherein the predetermined scheme specifies contiguous physical memory locations for the set of edge values.

13. A decoder according to claim 11, wherein the memory is partitioned according to degrees of the bit nodes.

14. A decoder according to claim 11, wherein edge values connected to bit nodes of n degrees are stored in a first portion of the memory, and edge values connected to bit nodes of greater than n degrees are stored in a second portion of the memory.

15. A decoder according to claim 11, wherein the structured parity check matrix imposes restrictions on a sub-matrix of the parity check matrix.

16. A decoder according to claim 11, wherein the LDPC coded signal is modulated according to a signal constellation that includes one of 8-PSK (Phase Shift Keying), 16-QAM (Quadrature Amplitude Modulation), 16-APSK (Amplitude Phase Shift Keying), 32-APSK and QPSK (Quadrature Phase Shift Keying).

17. A decoder according to claim 11, further comprising:
a Read-Only memory for storing addresses of the memory.

18. A decoder according to claim 11, further comprising:
a processor coupled to the memory, wherein the set of edge values is retrieved in a single clock cycle of the processor and is adjacent to a group of M bit nodes or M check nodes, where M is the number of parallel processing engines.

19. A memory accessible by a low density parity check (LDPC) decoder for decoding a LDPC coded signal, comprising:

a first portion storing a first group of edge values associated with a structured parity check matrix used to generate the LDPC coded signal, the first group of edges being connected to bit nodes of *n* degrees; and

a second portion storing a second group of edge values associated with the structured parity check matrix used to generate the LDPC coded signal, the second group of edges being connected to bit nodes of greater than *n* degrees, wherein a set of edge values from the first group or the second group is retrieved to output a decoded signal.

20. A memory according to claim 19, wherein the predetermined scheme specifies contiguous physical memory locations.

21. A memory according to claim 20, wherein the contiguous placement of edges imposes restrictions on the parity check matrix.

22. A memory according to claim 19, wherein the LDPC coded signal is modulated according to a signal constellation that includes one of 8-PSK (Phase Shift Keying), 16-QAM (Quadrature Amplitude Modulation), 16-APSK (Amplitude Phase Shift Keying), 32-APSK and QPSK (Quadrature Phase Shift Keying).